Void defect generation for BGA defect inspection

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The Ball Grid Array (BGA) technology is surface mount chip packaging technology that uses a grid of solder balls as its connectors. The benefits of BGA are: reduced co-planarity problems; reduced placement problems; lower profile; better electrical performance and higher interconnect density. However, BGA is not without the problems. The voids are one of the critical defects which cause reliability problems. The usage of lead-free solder results in increasing number of voids because of the higher surface tension and higher processing temperature. Therefore, fast and accurate void inspection with optimal inspection condition becomes key technology to manufacture high quality electronics. X-ray inspection is considered as the promising method for void inspection. In order to figure out optimal inspection conditions for critical sizes and locations of voids, it is essential to prepare the samples with various void sizes and formed location in BGAs. We performed flow simulations to figure out the void generation mechanism to make standard voids samples with intended sizes at given locations. Lead-free solder (Sn 96.5- Au 3.5) with 450μm Cu pad is used for modeling. The simulation results show that location of void is strongly dependent on the position of initially-formed void with this simulation condition. The center of finally-formed void is almost the same position where the center of initially-formed void was located in both vertical and horizontal direction. Also, there is no significant change in void size. In order to form a void between the solder bump and Cu pad surface, the bottom of initial void should pass through to Cu surface. It is expected that standard void sample with various sizes and location in bumps will help to figure out optimal inspection condition with respect to its size and location.

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1. Introduction

Flip chip technology is one of the promising methods to meet the functions of IT devices such as high-end mobile gadgets. Flip Chip (FC) process is the method to connect die to the substrate electrically by flipping the die. The interconnection between the die and substrate is made through Ball Grid Array (BGA) which is an array of metal balls for external electrical interconnection.

The voids in the solder joints are one of the critical defects that cause reliability problems. Voids may not only weaken mechanical joint strength but also degrade conducting performance. Various factors are responsible for the voids. Several reported causes of voids are as follows: (1) trapped flux that has not enough time to be released from the solder paste; (2) contaminants on improperly cleaned circuit boards; (3) void in original solder ball; (4) solder shrinkage during solidification; (5) moisture ingress to the solder materials; (6) vias in pad expelling a trapped air volume during reflow.

The adoption of lead-free solder is also the main factor that results in an increase number of voids. Physical differences between SAC (Sn-Ag-Cu) and SnPb contribute to void formation. Because SAC alloys have a higher surface tension than SnPb alloys, gasses that may become trapped do not escape as easily from the molten SAC alloy as they do from the molten SnPb alloy. Also, the higher processing temperature for lead-free solder is another cause for void. The elevated melting temperature of lead-free materials release more volatile compounds from the substrate and components. In addition, SAC materials have the decreased wetting characteristics which results in a larger wetting angle. The larger wetting angle means that any void that forms must travel a further distance to escape.

Voids can be found in a BGA solder ball, in the solder joint to BGA interface or in the solder joint to printed circuit board interface. IPC-610D and IPC-7095A are industry specifications for voids in BGA solder joints. For example, IPC-610D indicates that the total void percentage level within BGA solder balls should be less than 25 %. IPC-7095A has tighter values compare to IPC-610D. However, the size limitation criteria are defined by occupied percentage of void compare to solder bump area and differ in accordance with chip makers. Also, voids can be or cannot be critical defects according to outbreak locations.

It is essential to develop fast and accurate void inspection to

realize highly reliable electronics manufacturing. X-ray inspection method is non-destructive testing method which can penetrate the target to image the hidden void defects. In order to figure out optimal inspection conditions for critical sizes and locations of voids, the standard samples with various void sizes and formed locations in BGA solder are needed. We performed flow simulations to figure out the void generation mechanism to manufacture standard voids samples with intended void sizes at given locations. Different heat-transfer conditions on solder bumps with various initial voids were applied to ensure controllability of void size and location for standard void generation.

2. Void generation simulation

2.1 Initially-formed void on Cu pad: Heat transfer from Cu pad

2.1.1 Simulation model

As mentioned before, there are numerous factors causing the formation of voids. However, it is very difficult or impossible to simulate these factors, such as flux behavior, effect of contamination and moisture ingress effect. In my previous study, flow simulation analysis was carried out to find void formation mechanism when initially-formed dimples or voids are located in the solder bump surface and face-down to Cu pad interface. I found that the generation of finally-formed voids after reflow was closely-linked to the sizes and locations of initially-formed voids in solder bump surface. However, it was difficult to machining initially-formed void with expected size in a solder bump surface and keep the machined face down to Cu pad for reflow process.

We propose the model to form initially-formed void in the Cu pad to generate void defects in solder bumps with intended sizes and location. Fig. 1 illustrates one of the simulation models used for flow analysis. Initially-formed void size in Cu pad will vary. The voids on Cu pad with depth of 10 μm and width of 20 μm, 30 μm and 40 μm are utilized for simulation. Lead-free solder ball (Sn 96.5- Au 3- Cu 0.5) with diameter of 300 μm is located on 450 μm Cu pad. Initially-formed scratch is designed to locate on Cu pad just below solder bump.

Two-dimensional models with about 8,000 spatially uniform meshes are generated. Physical properties of solder ball used in simulation are summarized in Table. 1. Simulation conditions are listed in Table. 2. Heat is transferred from the bottom of Cu pad to the solder bump.

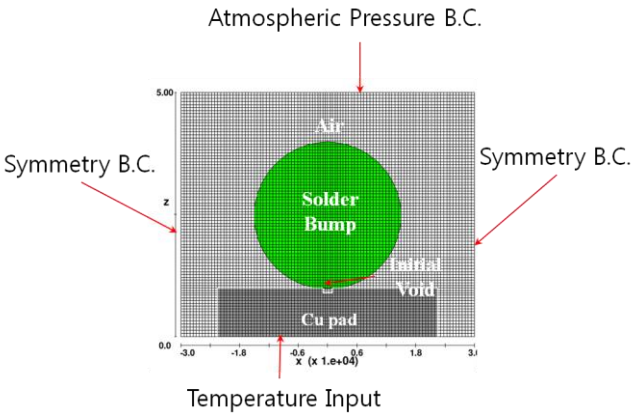

Fig. 1 Simulation model: initially-formed void on Cu pad

Cu pad is heated from 488 K to over liquidus temperature of solder (503 K) and then cooled below solidus temperature of solder (488 K) again. Atmospheric pressure of 101,325 Pa is assigned for initial pressure condition.

Table. 1 Physical properties of Sn 96.5-Ag 3-Cu 0.5

Parameter	Value [units]
Density of molten solder	7100 [kg/m^3]
Viscosity of molten solder	0.002 [Pa·sec]
Heat transfer coefficient	73 [W/(m^2·K)]
Specific heat	222.1 [J/(kg·K)]
Liquidus temperature	493 [K]
Solidus temperature	490 [K]
Contact angle of solder	80 [°]

Table. 2 Simulation conditions

Parameter	Value [units]
Initial temperature of solder	488 [K]
Initial temperature of air	298 [K]
Initial pressure	Atmospheric Pressure 101,325 [Pa]
Heat input	0 sec : 488 [K] 0.1 sec : 503 [K] 0.2 sec : 503 [K] 0.3 sec : 488 [K]

2.1.2 Simulation results

Simulated void growth and deformation of 300 μm-diameter solder ball on Cu pad with the depth of 10 μm and the width of 20 μm scratch is given in Fig. 2. Heat is transferred from the bottom of Cu pad to the solder bump. The simulated void growth and deformation of solder bump with respect to time interval is illustrated in order.

The temperature distribution is given in pseudo-color scale and arrows indicate flow direction. It is shown that the finally formed void is located in vicinity of the initial void location. The similar phenomenon was observed even the width of scratch is changed to 30 μm and 40 μm. It is expected that voids between solder bump and Cu pad interface can be generated using these conditions. The possible disturbance for X-ray void detection can arise from the initially-formed scratch in Cu pad. However, it can be reduced by using energy subtraction method. Even this void forming condition is applicable to generate void in vicinity of Cu pad, the location of void cannot be controlled.

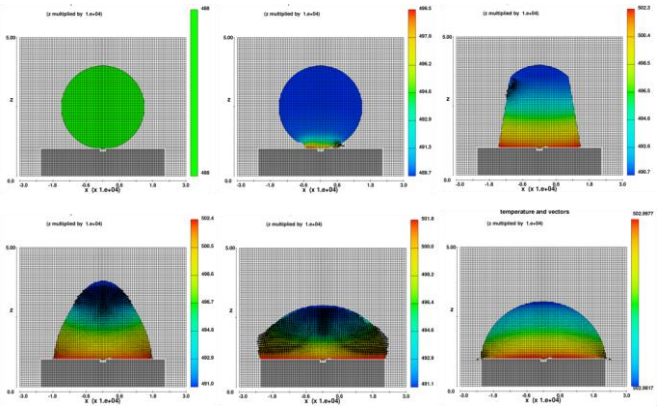

Fig. 2 Simulated void growth and deformation of solder bump (Initially-formed void on Cu pad)

2.2 Initially-formed void in solder bump: Heat transfer from Cu pad

2.2.1 Simulation model

We also propose the models that solder bumps with various sizes and locations are formed in solder bumps. The solder bumps can be manufactured by plating or screen printing, polishing and etching process in real world. It is expected that the location of void can be controlled by the location of initially-formed void in a solder bump while the model with initially-formed void in Cu pad only form void in the vicinity of Cu pad. Fig. 3 shows the simulation model of solder bump with initially-formed void in it. Lead-free solder bump (Sn 96.5- Au 3.5) with height of 300 μm and width of 450 μm is used for simulation. The area of solder bump is corresponding to 400 μm-diameter solder ball.

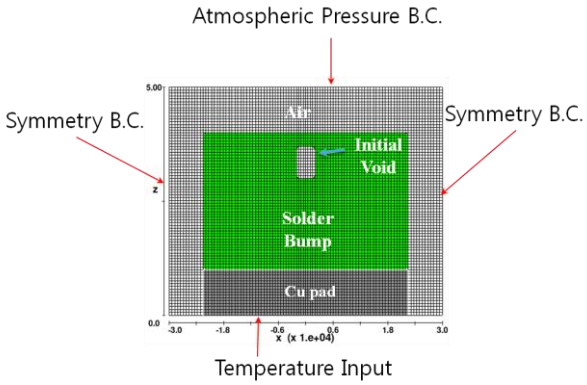

Fig. 3 Simulation model: initially-formed void in solder bump

2.2.2 Simulation results

In Fig 4, the simulated void growth and deformation of solder bump with respect to time interval are shown when the initial rectangular-shaped void with height of 70 μm and width of 40 μm is located in a solder bump.

Heat is transferred from Cu pad to the solder bump and the bump is melted from bottom to the top. The initially-formed void is pushed upward because melting process is proceeding from the bottom while the top of the solder bump remain in solid phase. Several simulations using different initially-formed void models were carried out. The same phenomenon is shown regardless of initially-formed void sizes and locations. These results imply that location control of void is difficult resulting from heat-transfer direction.

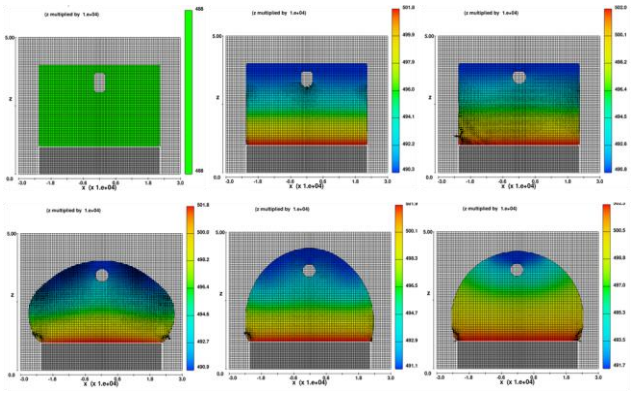

Fig. 4 Simulated void growth and deformation of solder bump (height: 70 μm, width : 40 μm)

2.3 Initially-formed void in solder bump: Molten condition

2.3.1 Simulation model

We found that heating condition is also one of the factors that influence the formation of voids from the previous simulation results. Therefore, we simulated heat condition under convection reflow in order to control the size and location of void. Convection reflow is a heat transferring method by means of heat radiation using fan to force heated air towards the chips from all directions. Accordingly, it is possible to assume solder bump is liquid state because heat is transferred from all directions and melting time is short. Initially-formed voids with various sizes of height and width which is located 30 μm below from the top of the solder bump. The same lead-free solder bump (Sn 96.5- Au 3.5) material and the same boundary condition are applied except heating condition. Surface tension of molten solder is set to be 0.431 N/m. The same physical properties listed in the previous clause are used for Sn 96.5 - Ag 3.5.

2.3.2 Simulation results

Fig. 5 illustrates one of the flow simulation results using initially-formed rectangular-shape void. The void has height of 70 μm and width of 20 μm which is located 30 μm below from the top of the solder bump. Void changes its shape to round and located almost the same position where the initially-formed void was located because the high viscosity of molten solder. Also, there is no significant change can be found in void size.

Similarly, the simulated results when the same-sized initial void is located 140 μm away from the center are given in Fig. 6. The similar phenomena were observed from this case, too. However, when the horizontal location of void from the center is about 1/3 of Cu pad width, the void is blown away.

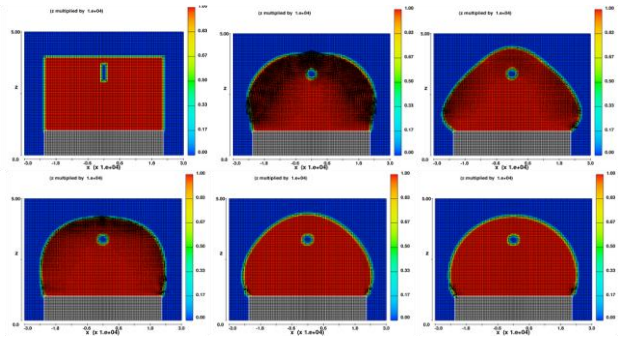

Fig. 5 Simulated void growth and deformation of solder bump (Initially-formed void height: 70 μm, width: 20 μm)

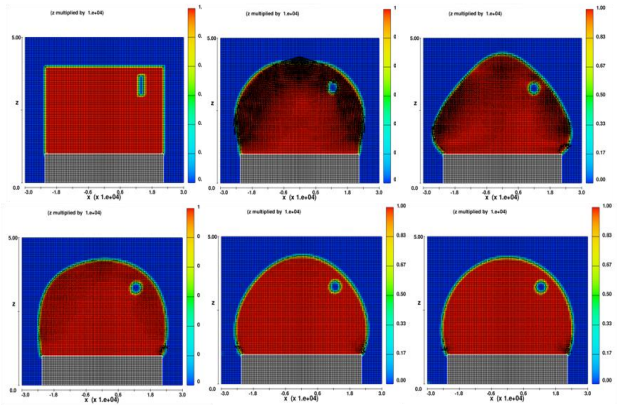

Fig. 6 Simulated void growth and deformation of solder bump (Initially-formed void height: 70 μm, width: 20 μm, 140 μm shifted from center)

Also, the bottom of initial void should pass through to Cu surface in order to form a void between the solder bump and Cu pad surface as shown in Fig.7. Numerous simulation results with various sizes and location of initially-formed void showed similar tendency. It shows the possibility of size and location control of voids.

Solder bumps with initially-formed void are in the process of production for feasibility demonstration. The solder bump sample can be generated by plating and etching process. Also, screen printing can be utilized instead of plating because plating can be time consuming process when target object has several hundred of micrometer in height.

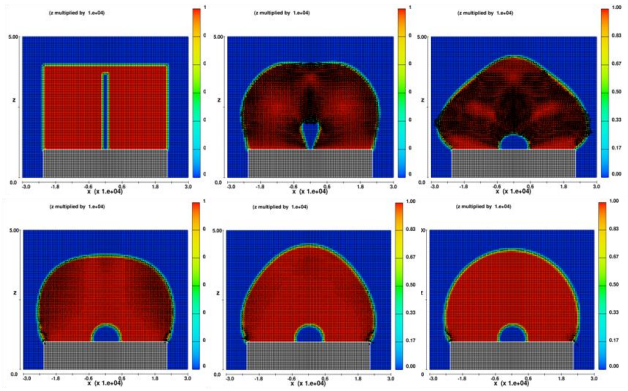

Fig. 7 Simulated void growth and deformation of solder bump (Initially-formed void height: 270 μm, width: 20 μm)

3. Conclusions

The voids are one of the critical defects which cause reliability problems in semiconductor chips. Generation of standard void sample is important to figure out optimal conditions for void defect inspection in BGA solder bump. In order to generate void samples with various sizes and locations in bumps, we suggested manufacturing voids intentionally in the bumps and reflow them to make intended void sizes and locations in bumps. Flow simulations were carried out in order to find the relationship between initially-formed void and finally formed one after reflow process. The influence of heat addition condition for several void defect models is also tested.

Basically we tested two defect models to generate intended sizes and locations of void. One is initially-formed scratch in Cu pad. The other is initial void in solder bump. Simulation results showed that the simulation model which has initially-formed scratch in Cu pad can generate void at solder and Cu pad interface. However, the location of void is difficult to control. We also tested the effect of heat-transfer direction with void defect model which has initially-formed void in the bump. We found that heat transfer from the bottom of Cu pad pushed the initial void to the upward from simulation results. In order to control the location of the void, uniformly heated condition is considered instead of heating from Cu pad. We can assumed that the solder bump is in molten state when the bump is small enough and instantly heated from all directions which can be achieve by convection reflow process. The simulation results show that location of void is strongly dependent on the position of initially-formed void with this simulation condition. The center of finally-formed void is almost the same position where the center of initially-formed void was located in both vertical and horizontal direction. Also, there is no significant change in void size. The bottom of initial void should pass through to Cu surface in order to form a void between the solder bump and Cu pad surface.

To verify feasibility of our proposed method, the samples with the solder bumps with initially-formed void is in the process of production using screen printing and etching process. It is expected that standard void sample with various sizes and location in bumps will help to figure out optimal inspection condition with respect to its size and location.

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