Precision dimensional metrology on 3D packaging process

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3D semiconductor packaging process, one of the next generation semiconductor processes, requires novel metrology to measure geometrical thickness and refractive index of a silicon wafer, depth of high aspect ratio holes, and multiple layers of wafers with nondegrading visibility. For geometrical thickness measurement and TSV measurement, the spectral resolved interferometers were suggested based on the optical comb for high speed measurement. To maintain the visibility for weak reflected light, visibility enhanced interferometer was proposed and realized based on an injection locking technique. These methods are expected to be useful for future packaging processes as well as precision inspection of 3D packaged circuits.

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1. Introduction

3D semiconductor packaging has emerged as one of the next generation semiconductor processes. Conventional semiconductor manufacturing based on optical lithography has a limit to make narrow linewidths due to the diffraction limit of light. Since diffraction limit is a function of the wavelength of light used, EUV is proposed as a new light source for narrow linewidth lithography while new semiconductor packaging methods have been studied whose strong candidate is to stack multiple wafers vertically to increase the density of the circuits. In semiconductor packaging process, there are high demands on new dimensional metrology. Firstly, the geometric layer thickness of each wafer must be accurately measured to build up multiple layers, while the refractive index of a silicon wafer should also be measured. With conventional optical interferometry it is difficult to separate the two quantities of geometrical thickness and refractive index from the optical thickness. Secondly, holes having high aspect ratio such as through silicon vias(TSVs) are to be measured. TSVs which are vertical electrical holes through a wafer, can connect stacked wafers together electrically. The depth of these holes are difficult to measure by existing optical methods such as white-light scanning interferometry and confocal microscopy because light cannot penetrate through deep holes, and is diffracted at the edges of the holes. Thirdly, the reduced light which is reflected from the lower layers through the silicon wafer stack causes poor visibility to the inference fringes when using optical interferometry. To measure the inside of multiple layers the visibility should be improved, which can be solved typically by adjusting and matching the intensities of lights in the reference arm and the test arm. However, the amount of light to be adjusted in the reference arm has to be changed whenever the wafer under measurement is located in a different layer in the wafer stack because the reflectivity of light depends on the number of layers existing upon the wafer of interest.

In this paper, three new measurement techniques for semiconductor packaging process are covered; (1) geometrical thickness and refractive index of a silicon wafer measurement, (2) TSV depth measurement, and (3) visibility improvement for multiple layers measurement. Spectral resolved interferometer based on the optical comb was adopted for inline high-speed traceable measurement, and uncertainty analysis was performed to ensure the measurement reliability. The suggested methods are expected to be used for next-generation semiconductor packaging production and process development.

2. Dimensional metrology for 3D packaging process

2.1 Geometrical thickness and refractive index measurement

Spectral resolved interferometer can measure distance by analyzing optical spectrum of interference signal in wide spectral bandwidth. The period of the obtained spectrum gives the optical path difference between two interfering beams. An optical comb having the spectral range of 1535 nm to 1555 nm with a repetition rate of 25 GHz was adopted as a light source. Figure 1 shows the optical layout of the measurement system consisting of a Michelson type interferometer constructed to separate the geometrical thickness and refractive index of a silicon wafer from the optical thickness. Four optical path differences, A, B, C and D were obtained from ray 1 and ray 2 at the same time. The optical path differences,

A = (L1 + T + L2)-L0, B = L1-L0, C = (L1 + N・T)-L0 and D = (L1 + N・T + L2)-L0 are expressed in terms of L0, L1, L2, T and N. Geometrical thickness and refractive index were determined by T=(C-B)-(D-A) and N=(C-B)/T, respectively. In 10 repeated measurements, the geometrical thickness of the silicon wafer was found to be 334.85 ㎛ with the standard uncertainty of 0.95 ㎛ (*k*=1). The refractive index of the silicon wafer was measured as 3.50 [1].

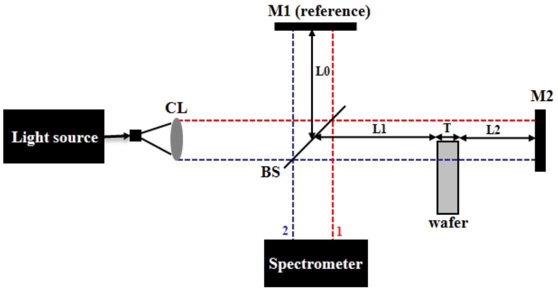

Fig. 1 Optical layout of a spectral resolved interferometer for measuring geometrical thickness of a silicon wafer (CL: collimation lens, BS: beam splitter, M: mirror, T: thickness of a silicon wafer, N: refractive index of a silicon wafer, L0: distance between BS and M1, L1: distance between BS and the front surface of a silicon wafer, L2: distance between the rear surface of a silicon wafer and M2)

2.2 TSV measurement

Depth measurement of a large aspect ratio hole such as TSV based on conventional optical measuring methods is not an easy task because the light cannot penetrate into deep holes with very small diameter. Infrared light can be used to measure the depth of TSVs because it can partially pass through a silicon wafer. Based on the spectral resolved interferometry, the vertical depth was measured in a single measurement without any mechanical scanning. Fig. 2 shows FFT results of the spectrums obtained at locations with and without a TSV. In this task, the depth of TSVs with 25 ㎛ diameter was measured as 133.1 ㎛.

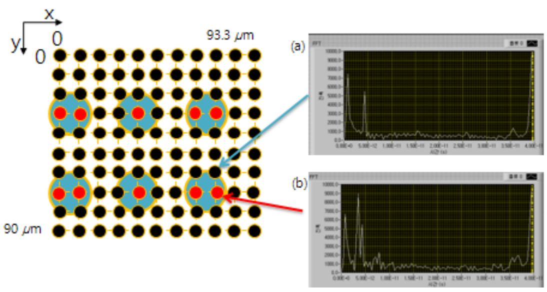

Fig. 2 FFT results of the spectrums obtained at two locations (a) with a TSV (b) without a TSV

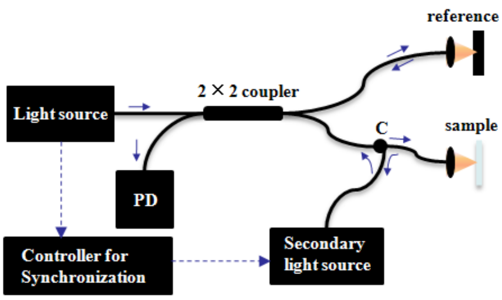

Fig. 3 Optical layout of the VEI (PD: photo detector, C: circulator)

2.3 Visibility enhanced interferometer, VEI

The best visibility can be observed when the intensities of light reflected from a reference mirror and a target are equal. Generally the intensity of the light reflected from a given reference mirror is constant. However, the intensity of light reflected from the target may vary according to the reflectance, surface roughness and shape of the target. Therefore, the visibility is degraded when the light pass through multiple layers. To avoid the problem, the light reflected from the reference mirror should be adjusted whenever the condition of the target changes. Visibility enhanced interferometer was suggested to avoid the degradation of the visibility regardless of the condition of the targets. Figure 3 shows the optical layout of the VEI. The basic principle of the method is to amplify the reflected light from the target to the same level as the reference light without any phase distortion. It can be realized by synchronizing a secondary light source with a light source based on the injection locking technique. In our experiments the high visibility could be maintained even when the reflectance of the target was only 0.06 % [2].

3. Summary

To meet new metrological demands on 3D packaging processes, three different measurement techniques of (1) silicon wafer thickness and refractive index measurement, (2) TSV depth measurement and (3) VEI for multiple layers were proposed and implemented. It is expected that they will be useful for the future 3D packaging processes as well as precision inspection of 3D packaged circuits.

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