Signal detection of multi-channel capillary electrophoresis microchip based on CCD

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KEYWORDS : Capillary electrophoresis, CCD, FPGA, SOPC

A kind of multi-channel capillary electrophoresis (CE) signal detection system based on CCD is described. The output signal data of the CCD sensor were processed by a series of pre-processing circuits and ADC, then it was collected by the Field Programmable Gate Array (FPGA) board which communicated with host computer. The core in FPGA was designed to control the signal flow of the CCD and transfer the data to PC based on a Nios II embedded soft-processor. The customer application of PC was used to store the data and demonstrate the curve. The experiment results shown that this multi-channel capillary electrophoresis chip detection system could detect different intensity fluorescence signal in each channel at the same time, and the results could be displayed on line.

Manuscript received: January XX, 2011 / Accepted: January XX, 2011

NOMENCLATURE

CCD=charge coupled devices
CE = capillary electrophoresis
FPGA= field programmable gate array
SOPC = system on programmable chip.

1. Introduction

Lab on a chip has been rapidly developed recently [1-3]. All the instruments can be incorporated into a small chip achieving sample pretreatment and high throughput analysis. Among many applications of lab on chip, the microchip capillary electrophoresis has become an accurate and efficient analytical technique, which was widely used in genome sequencing project, epidemic diseases testing, blood and drug screening. With the life science development more and more samples need to be analyzed, therefore a kind of high-throughput capillary electrophoresis detection system should be developed [4-7].

A multi-channel capillary electrophoresis with laser induced fluorescence detection system based on CCD was presented in this paper. FPGA chip was selected as the core of the hardware circuit, the driver for circuit module and A/D converter module were designed with Verilog HDL on Quartus II software platform. The output signals of CCD were processed by a series of pre-processing circuits and A/D chip, then the signal was collected by the FPGA board with the core of an embedded Nios II software processor and transferred to host computer [8]. The detection curve was shown on the host screen. There were two software parts for the detection system. One was the soft core in FPGA, which was designed to receive the signal of the CCD and send the data to PC. The other one was an application on host based on Visual C++, which was used to process and show the detection result.

2. Structure of detection system

A typical experimental detection system for the CE chip with CCD linear image sensor was shown in Fig.1. The beam from the semiconductor laser was positioned in the micro channel. The sample was driven by the high-voltage power through the detection point, the fluorescence was excited and captured by the CCD. The signal data from the CCD was pre-processed by the FPGA board and picked up by the host computer.

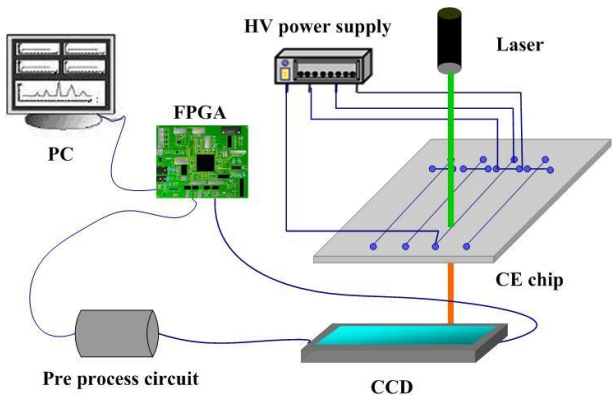


Fig. 1 Structure diagram of the detection system

FPGA is the main logic controller and generate the driving timing pulse for the CCD in this system. The analog signal from the CCD sensor through the differential, filter and amplifier circuit was sent to the A/D chip TLC5510. The digital pixels-signal was processed by the FPGA chip along with the embedded Nios II processor, and the data was transferred from the hardware board to the host computer via RS232. The hardware architecture is shown in Fig. 2.

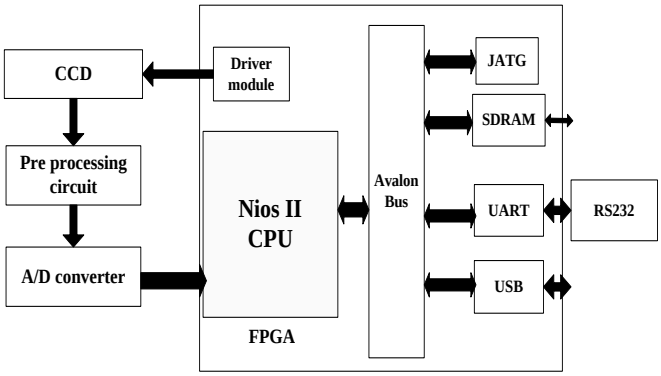


Fig. 2 Basic architecture of hardware

2.1 CCD driver module

TCD1208AP fabricated by Japan TOSHIBA Company was selected as the CCD sensor, which is a high sensitive and low dark current 2160-element image device. Image sensing element size is 14μm by 14μm, the over length is 30.2mm. Because the microfludic channel width of the capillary electrophoresis chip is 100μm; the distance between the two micro channels is 6mm, the sensor element size is large enough that can complete the detecting.

The driver module of the FPGA chip produced the clock for the CCD according the time sequence which was designed with schematic composer as shown in Fig.3. The pulse of light integral SH and the charge transfer pulse CR1 and CR2 was set up by the software in the counter mode. The clock cycles could be adjusted by the counter according the CCD drivers. The input clocks determined all the output pulse, but they were mutually independent actually and the SH with RS avoided the race and hazard.

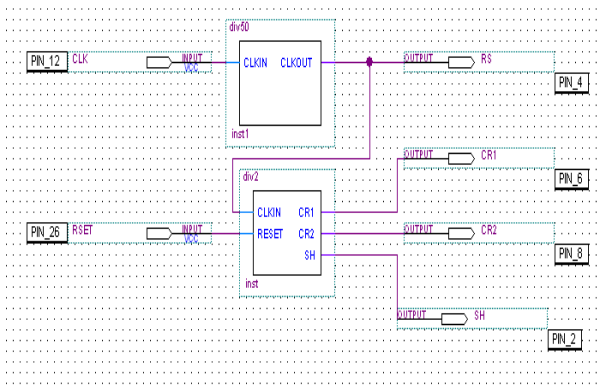


Fig.3 The schematic of CCD driver

The clock frequency of signal CLK was 50MHZ and the working frequency of CCD was 1MHZ, so the module Div50 divided the CLK by 50 and produced the reset signal RS which duty ratio was 1:3. The module Div2 divided the RS by 2 that produced the two phase pulse CR1 and CR2. Their frequency was 0.5MHZ, the duty ratio was 1:1. The SH controlled the output signal frequency of the CCD. The simulation waveform is shown in Fig.4. As can be seen，the width of the wide pulse of the CR1 and CR2 is larger than the SH signal pulse which pulse number is more than 1106 in one cycle.

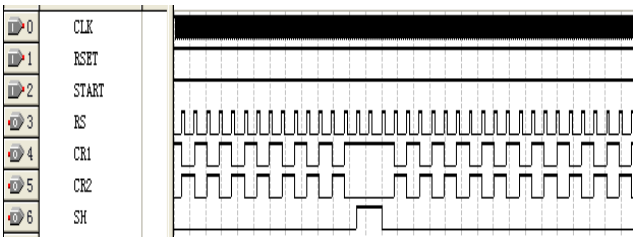
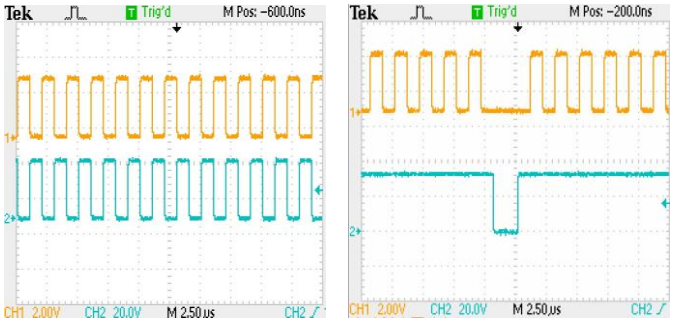


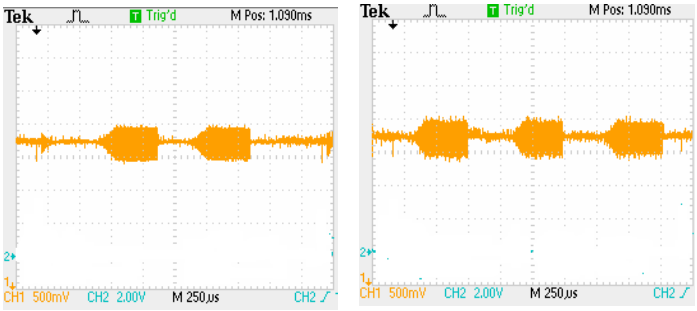
Fig.4 Simulation waveform of CCD driver

Finished the device configuration, the code was compiled and downloaded into the FPGA chip under the Quartus II development environment. The output waveform of the pins are shown in Fig.5 by the DSO (Digitizing Storage Oscilloscope), the wave meet the phase and amplitude requirements of the CCD. Using the 532nm laser as the light source, a black film with different number slits was covered on the CCD sensor, the slits were transparent and distances between them were similar with the micro channels. The waveform detected by CCD as shown in Fig.6, it demonstrated that CCD driver module could make sure the TCD1208AP chip work normally.



(a) Charge transfer pulse CR1,CR2 (b) The pulse of SH and CR1

Fig.5 Driving waveform on DSO



(a) The film with 2 slits (b) The film with 3 slits

Fig. 6 Signals on DSO with different slits

2.2 Differential circuit

TCD1208AP CCD sensor has two outputs which contain noise caused by the reset pulse RS. In order to get effective signal, the noise of the compensation output (DOS) and the signal output (OS) can be eliminated by the differential amplification circuit. The AD620 was selected as the reverse amplification which could reduce interference as shown in Fig.7. The AD620 is a low cost, high accuracy

instrumentation amplifier that has a wide input voltage scale (±2.3 to ±18V), high CMRR(100dB), low input noise(below 0.28μV), over voltage protection and low drift potential etc, and requires only one external resistor to set gains between 1 to 10,000.

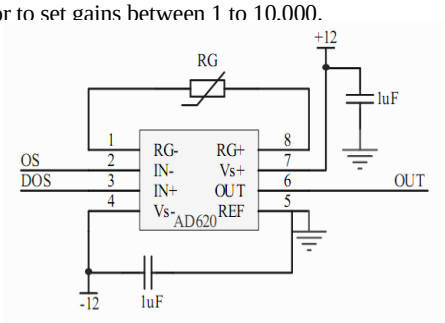


Fig.7 Differential circuit

2.3 Filter circuit

The output signal of the CCD was imposed with high-frequency noise, so a low-passed filter was used to get the accurate value. The voltage-controlled voltage source (VCVS) low-passed filter was employed as shown in Fig.8. It was composed of RC filters and a proportional amplifier. According the VCVS second order low- pass filter, the cutoff frequency is

$$f_o = \frac{1}{2\pi\sqrt{R_{37}R_{38}C_{63}C_{64}}}$$

Based on the Nyquist Sampling Theory, the cutoff frequency was adjusted. While it was same with the frequency of the reset pulse, the noise could be reduced well, the parameters were designed as C_{63} = C_{64} =100pF, R_{37}=R_{38}=1.6kΩ.

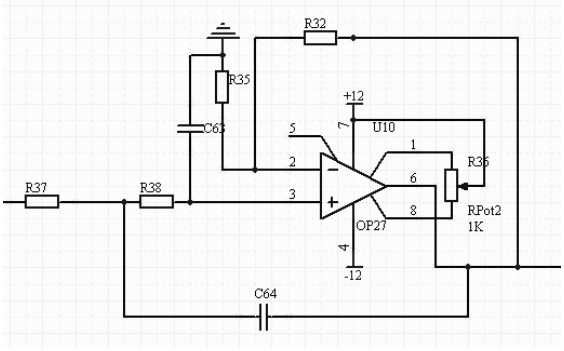


Fig. 8 VCVS second-order low-pass filter

2.4 Voltage amplifier

The linear CCD is a low power device and the output signal is weak. The AD620 could not amplify the voltage of the signal, so the output signal should be processed by a voltage amplifier circuit as shown in Fig.9 before the signal was send to A / D converter.

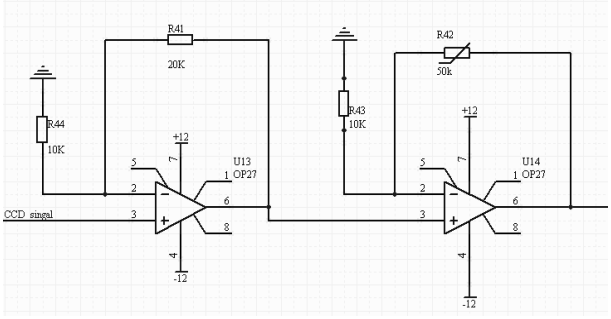


Fig. 9 Voltage amplifier circuit

2.5 A/D conversion

To realize high speed sampling, TLC5510 was chosen as the analog digital converter which is Texas Instruments (TI) produced eight half-flash ADC structure, can provide minimum 20Msps sampling rate. It has internal sample and hold circuit, which greatly simplifies the design of the external circuit as shown in Fig.10. Driving pulse CLK for A/D converter is generated by FPGA chip. The light integral SH of CCD pulse controls the OE of the ADC to achieve the video signal output and synchronizes the digitizing process. The 8-bit digital signal was transmitted to the FPGA through the D1-D8.

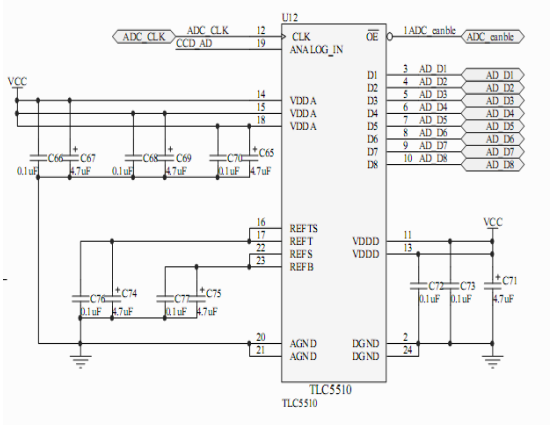


Fig.10 TLC5510 peripheral circuit

3. Software architecture

3.1 Embedded system design

The architecture proposed in the system was realized as a system-on-programmable-chip. The system-on-chip (SOC) is a self contained chip that holds all the necessary hardware and electronic circuitry for a complete system. The embedded system is assembled by means of the SOPC tool, using the library components and defining the interconnection. A controlling system was designed as shown in Fig.11 in SOPC builder of Quartus II development environment. The main unit of the system consisted with a Nios II processor, on-chip memory (RAM and ROM), peripheral inter-faces, I/O logic control, data converters and some Avalon slave components which are mapped to Avalon bus. Meanwhile, its respective address and interrupt requirement sequence number were generated automatically. The PLLs components for Nios II and the memory clocking were added [9-10].

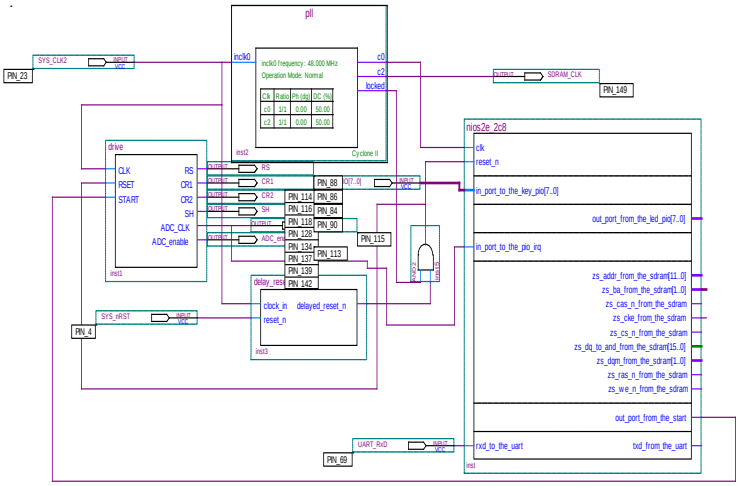


Fig.11 System of Nios II

The host PC sent the "Begin" command to the FPGA board, the Nios II soft core started the CCD driver and A/D conversion module and received digital pixel signal through the ADC produced by the CCD sensor. Each frame of the signal received by the FPGA chip was loaded into SDRAM memory buffer. When one frame was completed, the data was sent to the host computer and closed the driver with A/D module as shown in Fig.12. The procedure was repeated to capture the next frame. This program was written in C and downloaded to the FPGA board by Alter's Nios II IDE[11-12].

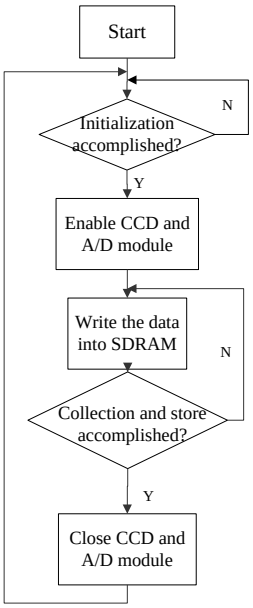


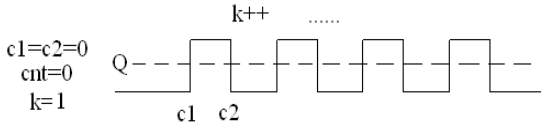
Fig.12 The flow of program in CPU

3.2 Host Applications

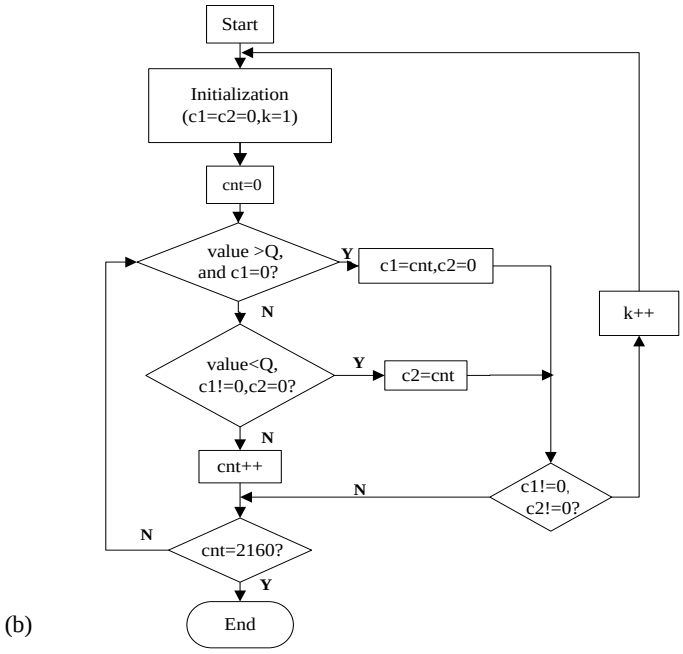
The application frame was designed by the App Wizard of the VC++, and the MFC application program was utilized to complete it. This data acquisition software provided a friendly man-machine interactive interface and realized such functions as data accept, signal processing, display and data store.

The CCD data from the FPGA board was put into the two dimensional array buffer [400][2160]. Each row stored one frame data and different row corresponded to different sampling times. For drawing the graphs, the data in array buffer need to be further proceed, including D/A, channel recognition and data sieving.

The channel recognition principle is shown in Fig.13. The Q is the pixel reference value; c1 and c2 are the pixel number of the two sides of the micro channel, the pixels data between c1 and c2 are the valid signal value in this channel. The channel number is k, cnt is counter increased by one which is triggered by rising edge of RS. The program will detect the all the pixel data with the increase of the cnt. When the value is higher than Q, c1 is given the current cnt number, if it is lower, c2 is given the cnt. At the beginning, the default value of k is 1, the default channel is No.1, after both c1 and c2 have value, the k increase 1, and turn to the next channel. Then repeat the step until the entire pixel was processed.



(a)



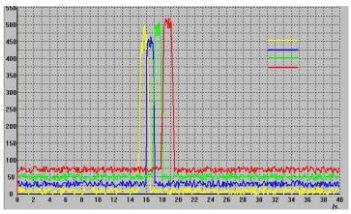
(b)

Fig.13 (a) The diagram of channel identification (b) The flow of program for channel identify

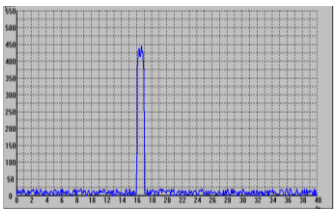
4. Performance

At the beginning, the CE chip was pretreated with deionized water and the running buffer. After the introduction of the sample solution, the voltage was applied across the micro channel in two steps: injection and separation, at the same time, the laser and FPGA board prepare to work [13-14]. While the sample moves to the detection point, the laser excites the fluorescence which was received by the CCD sensor.

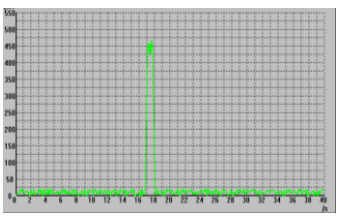
The signal data from the CCD was transmitted to the FPGA chip and through the UART-port to the windows XP based host computer. The signal data were captured by the PC and the results were displayed on the screen as shown in Fig.14. The interface could display not only the detecting curve of single channel but also the four channel curves at the same time. The signal peak of the channel 2, 3, 4 delay channel 1, because the laser scan from No.1 to other channel sequentially. The peak of the signal is distinct, it indicate that the detecting system has higher sensitivity and SNR. The testing parameters correspond to the practical situation.



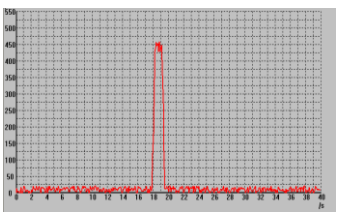
(a) The 4 channels signal together



(b) In channel 2



(c) In Channel 3



(d) In Channel 4

Fig.14 Fluorescence intensity vs. time(s) in different conditions

5. Conclusions

The design of a multi-channel capillary electrophoresis (CE) signal detection system based on CCD and FPGA was presented in this article. The FPGA chip is configured as a System On Programmable Chip with a Nios II soft processor in the system. The system controlled by the soft core provides more flexibility for processing and transferring of the CCD signal. The experiments demonstrated that various intensity of fluorescence signal in the capillary electrophoresis channel can be grabbed by the CCD and displayed by the host PC with the custom software on line. The results show that the detection system has the advantages of low cost, better stability and higher sensitivity compared with conventional confocal laser induced fluorescence detection system Future work will optimize the custom software and increase new module for specific application.

ACKNOWLEDGEMENT

The authors gratefully acknowledge the financial support of the National Natural Science Foundation of China (61074166).

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